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Transformer based equalisation circuit applied to n-number of high capacitance cells

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***Abstract* -- Over the last decade various high capacitance devices have become available on the market such as supercapacitors, ultracapacitors and recently, Li-ion capacitors. The cell voltage limit of each of these technologies is a small percentage of the system level voltage so they must therefore be connected in series to attain a high voltage. During charging and discharging, manufacturing tolerances between the cells result in voltage mismatch across the stack. Mismatched voltages are an inefficient use of the energy storage medium and can lead to dangerous failures in the cells if voltages exceed safety limits. Transformer based voltage equalisation techniques are the preferred circuit topologies in applications with low system voltage due to simplicity of control and low number of switches. The drawback of these circuits is the number of isolated windings which are required on a single core. This paper describes for the first time a solution to that problem by using a classical two windings transformer that in principal can be applied to any number of capacitors. The paper describes the operation of the circuit, shows simulation results and practical results based on a prototype with 5 cells.**

Keywords: Li-ion capacitor; Voltage Equalisation;

I. INTRODUCTION

High capacitance devices such as supercapacitors or hybrid capacitors have a high power density and cycle-life compared to battery technology. Supercapacitor technology is an excellent candidate for hybrid drivetrains (either using internal combustion engine or fuel cell power plants) in electric vehicles as they can provide the high dynamic response required for good acceleration and regenerative braking [1-3]. Besides electric vehicles supercapacitors have also been suggested in general electric drives applications [4, 5] as well as earth moving equipment [6], renewable generation [7], subways [8] and smart-grid/micro-grid applications [9-11].

In 2008 Li-Ion capacitors (made by JM Energy) became available onto the open market. Since 2009 the family of cells has grown and at the time of writing includes 1100F and 2200F pouch cells and 2300F and 3300F prismatic cells [12]. These hybrid cells have higher cell voltage and increased power and energy density compared to more traditional supercapacitor technology whilst maintaining the power density and cycle-life performance. With higher cell voltage, fewer series-connected cells are required to reach a given voltage. The Li-ion capacitor is therefore suitable (if not more so) for applications where traditional supercapacitors have been proposed as the energy storage system.

As with supercapacitor technology, manufacturing tolerances result in variation of the parameters of these cells such as capacitance and series resistance from cell to cell. For a series connection of cells (required to attain system level voltages) these mismatched parameters will lead to unequal voltages across the stack of cells. Operating the cells outside of their voltage range can lead to failure of cells whilst limiting charging when one cell reaches maximum voltage does not utilise the energy storage potential of the stack efficiently [13].

Whilst some simple systems exist for resistive cell discharging to attain equalisation these techniques are too inefficient for many applications and are not considered here. A number of equalisation scheme converters have been proposed in literature (inductor-less, bi-directional buck-boost, transformer based) which are, in theory, much more efficient than the resistive discharging methods. Detailed examination of these converters is beyond the scope of this paper, however, analysis of a representative sample of existing equalisation schemes can be found in another publication by the authors [14].

Two of the most common transformer based voltage balancing circuits are shown in Figure 1. Figure 1a shows the Flyback converter with distributed secondary windings and Figure 1b shows the Forward converter with distributed primary windings. Both converters were originally presented for the purposes of voltage equalisation in [13] and show significant performance advantages compared to the performance of inductor-less schemes and bi-directional buck-boost balancing circuits. In transformer based voltage balancing circuits the transformer provides galvanic isolation which is required for energy transfer between non-adjacent cells.

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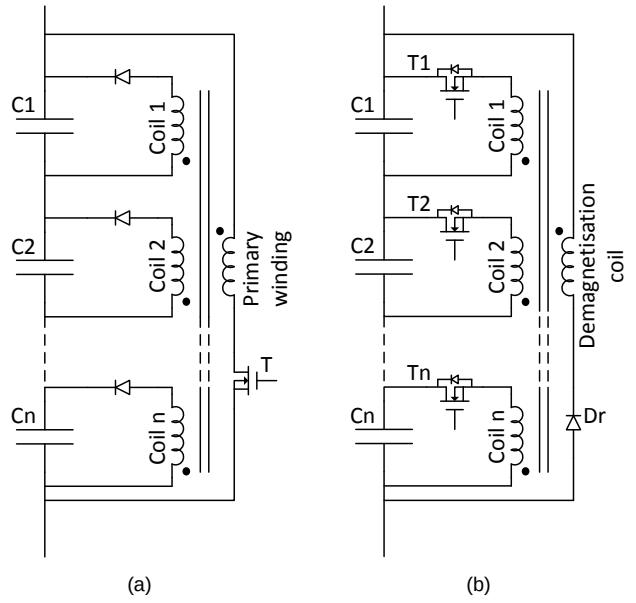

Figure 1 - (a) Flyback converter with distributed sencondary windings; (b) Forward converter with distributed primary windings

The Flyback converter with distributed secondary windings (Figure 1a) operates by deviating charging current from the stack into the primary winding and distributing the current in different levels according to the dispersion in voltage of the cells. The cell that has the lowest voltage will see the highest charging current. The advantage of this circuit is that it only requires one switch however the disadvantage is that during the period where the switch is in its on-state, current passes through all capacitor cells, therefore producing losses in each capacitor cell during the magnetization of the primary coil.

The Forward converter with distributed primary windings (Figure 1b) operates by selecting the cell to be discharged and charged. During the energy transfer the transformer stores and releases the energy depending on the switches selected. This circuit requires many more switches compared to the Flyback converter but allows greater flexibility of control.

The fundamental downside of the two circuits and similar transformer based circuits that have been published [15-24] is that the transformer requires separate windings for each capacitor cell. In a stack with many cells (typical systems may have hundreds of series connected capacitor cells) the design of the transformer becomes cumbersome and complex to construct. Replacing a multi-winding transformer with a classical two windings transformer would significantly simplify the complexity of the magnetic component. Therefore, a new converter topology is proposed utilising a multi-winding transformer with only two windings.

II. Proposed Converter Topology and Operation

Figure 2(a) shows the proposed equalisation converter for n-number of capacitors and Figure 2(b) shows the circuit for 5 capacitors. The converter consists of three parts: a solid-state power MOSFET multiplexer, a standard two windings transformer and a selector circuit. The solid-state MOSFET multiplexer comprises n+1 MOSFET pairs (S_1 to S_{n+1}), where n is the number of capacitor cells. MOSFETs in each pair are connected in a totem-pole arrangement and controlled by one control signal; thus both MOSFETs are either ON or OFF at the same time. The role of the MOSFET power multiplexer is to connect the cells that need to be discharged and charged to the rest of the equalisation circuit. The second part of the circuit is the transformer itself. A classical two windings transformer is used with coils wired in opposing polarity. The third part is the selector circuit that consists of four MOSFET switches; ST1a, ST2a, ST1b, ST2b. ST1a and ST1b are connected in a totem-pole arrangement ("1" indicates that both MOSFETS are connected to coil 1) and so are ST2a and ST2b ("2" indicates that both MOSFETs are connected to coil 2). Each selector MOSFETs is controlled independently. The selector switches are required to apply the correct winding (coil 1 or coil 2) to the capacitor cell for the energising and de-energising process. Figure 2 shows that each selector MOSFET has also anti-parallel diodes added. These diodes are added because they have lower on-state voltage than the body diodes of the MOSFETs.

It would be possible to replace the transformer and selector with an H-bridge arrangement – removing the second winding. However, the structure of the multiplexer would mean that each switch of the H-bridge would have to be bi-directional and losses would be higher thus this concept is not considered in this paper.

The equalisation scheme operates in four distinct periods. For simplicity the operation is explained on the five capacitor cells converter (Figure 2b) charging capacitor C3 from capacitor C1 (assuming that C1 has a higher voltage than C3). The four distinct periods are the magnetising period (Figures 3a & 4a) and the demagnetising period (Figures 3c & 4c), which are separated by the dead time period (Figures 3b & 4b). After the demagnetising period a non-conduction period applies (Figures 3d & 4d). The operation within each of the four periods is described below in more detail. The description assumes ideal components and a transformer ratio of 1:1. However, the internal resistances of the MOSFETs and diodes are included in the following discussion as they determine the rate of cell voltage change as shown later.

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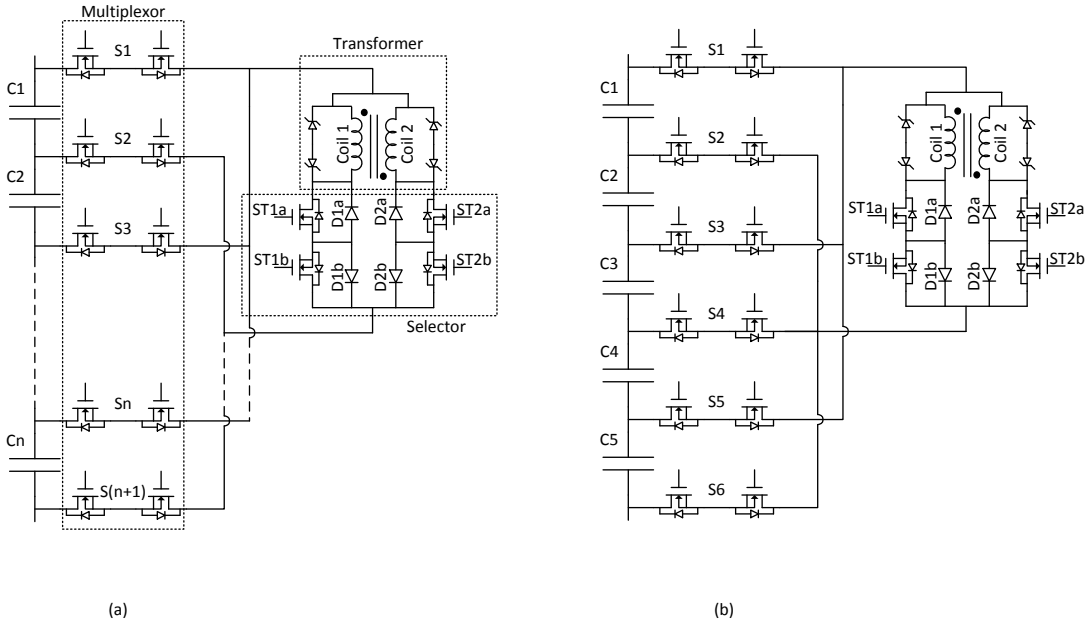

Figure 2 – Proposed equalisation circuit for (a) n-number of capacitors (b) 5 capacitors

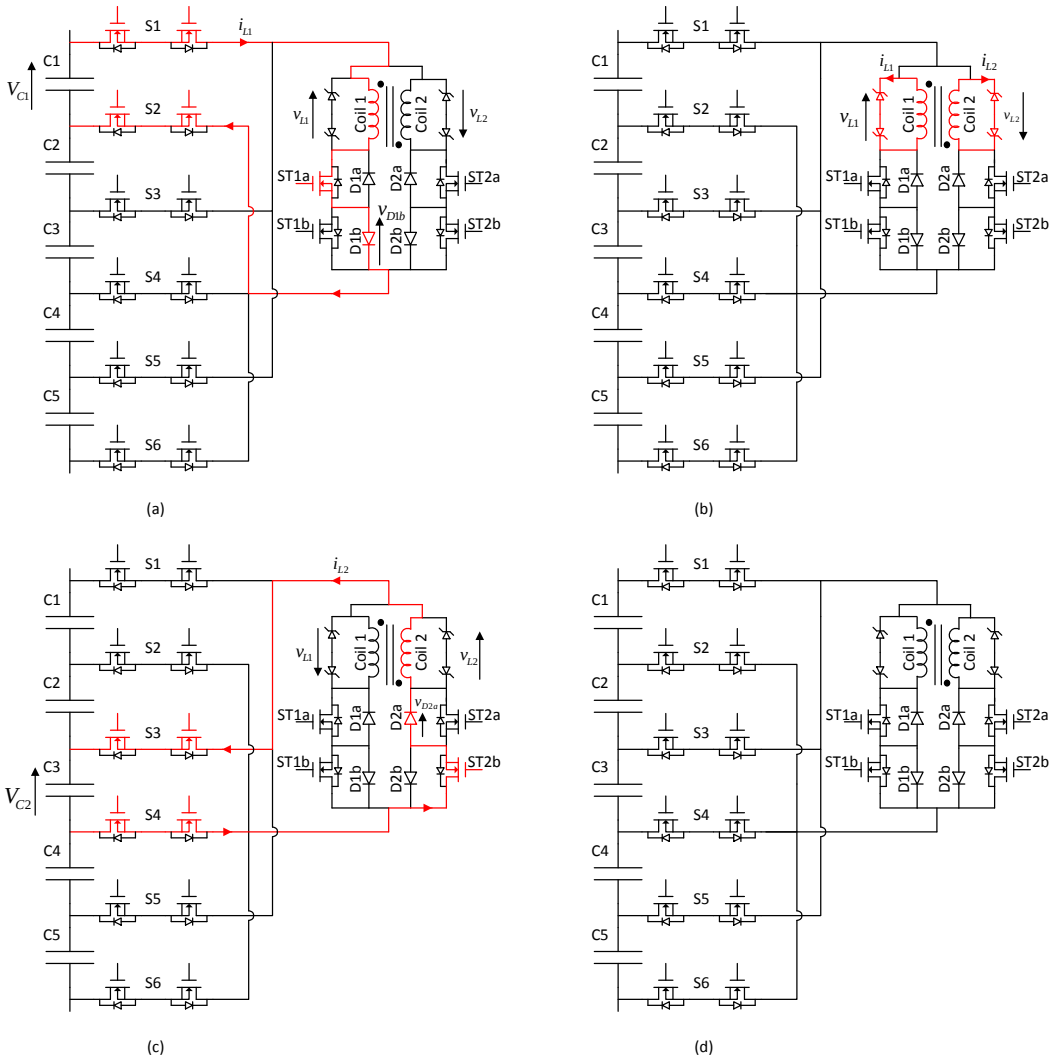

Figure 3 – Operational periods of the proposed converter based on a five cell converter and energy transfer from C1 to C3 showing (a) demagnetising period, (b) dead-time period, (c) demagnetisation period and (d) the non-conduction period

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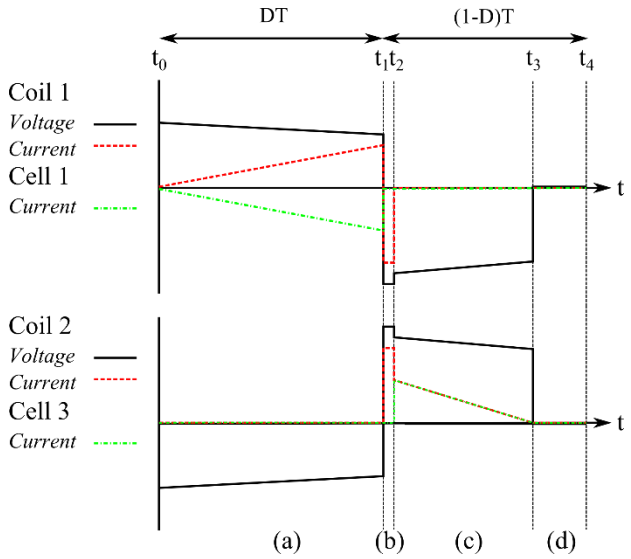

Figure 4 – Idealised transformer waveforms for energy transfer from capacitor cell C1 to capacitor cell C3 during (a) demagnetising period, (b) dead-time period, (c) demagnetisation period and (d) the non-conduction period

Period 1 – t_0 to t_1 – Magnetisation period

The source capacitor C1 is connected across coil 1 of the transformer via the two multiplexer switches S1 and S2, the selector switch ST1a and diode D1b. All devices are on for the entire magnetisation period.

In this arrangement the capacitor cell voltage V_{C1} of capacitor C1 is applied across the winding of coil 1 via the switches and current in the circuit in coil 1 begins to rise. The transformer voltages and currents can be derived and the equations are shown in (1) – (4), where $v_{L1}(t)$ and $v_{L2}(t)$ are the actual voltages across coil 1 and coil 2 respectively, $i_{L1}(t)$ is the positive current in coil 1 which is defined as per coil dot convention and $i_{L2}(t)$ is the current in coil 2, R_{ch} is the channel resistance of the individual multiplexer MOSFETs S1 and S2 and the selector MOSFET ST1a (for simplicity it is assumed that the channel resistance of all MOSFETs are the same), R_D is the resistance of the anti-parallel diodes in the Selector and L_1 is the inductance of coil 1.

$$v_{L1}(t) = L_1 \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \quad (1)$$

$$v_{L2}(t) = -L_1 \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \quad (2)$$

$$i_{L1}(t) = \frac{V_{C1}}{5R_{ch} + R_D}\left(1 - e^{-\frac{5R_{ch}+R_D}{L_1}(t-t_o)}\right) \quad (3)$$

$$i_{L2}(t) = 0 \quad (4)$$

The amount of energy that has been transferred into the transformer can be calculated with (5):

$$E = \int_{t_0}^{t_1} V_{C1} i_{L1}(t)\mathrm{d}t \quad (5)$$

Period 2 – t_1 to-t_2 – Dead time period

In order to transfer the stored energy from coil 1 to capacitor C3 the multiplexer switches S3 and S4 must turn on. However, before S3 and S4 can be turned on, S1 and S2 must be switched off otherwise a short circuit is produced between capacitor C1 and C2 as well as C2 and C3. Thus, in Period 2 switches S1-S4 are all off. The length of the dead time is determined by the turn-off time of the MOSFETs at maximum current level. For simulation and practical work a fixed time of 500ns has been identified as sufficient. In the dead time period voltage and current levels are assumed to remain constant.

During the dead time period both coils of the transformer become open-circuit generating an elevated voltage across coil 1 and also hence coil 2. In order to reduce the voltage peak a pair of Zener diodes has been added to each coil (Figure 2). Each pair is connected in an anti-parallel arrangement thus one Zener diode is forward-biased and the other Zener diode is reversed-biased for a coil voltage spike of either polarity. This arrangement clamps the voltages across the coils to a maximum value, V_{clamp}, in order to protect the switching devices.

The value of the clamp voltage V_{clamp} should be at least equal to the initial coil voltage level at the beginning of the demagnetisation process. In practice the initial coil voltages vary with the sink capacitor voltages. Therefore a clamp voltage value of twice the maximum rated capacitor voltage is sufficient. The Li-ion capacitors used in this project had a maximum voltage of 3.8V resulting in a clamp voltage of 7.6V. Since Zener diodes are available in discrete Zener voltages the diode used has next Zener voltage up; 8.2V.

With a clamp voltage of 8.2V and assuming that each Zener diode has the same internal resistance when conducting in both forward and reverse the winding currents and the coil voltages during the dead-time period can be written as:

$$v_{L1}(t) = V_{clamp} \quad (6)$$

$$v_{L2}(t) = -V_{clamp} \quad (7)$$

$$i_{L1}(t) = -\frac{V_{clamp}}{2r_{Zener}} \quad (8)$$

$$i_{L2}(t) = \frac{V_{clamp}}{2r_{Zener}} \quad (9)$$

Although in this period there is conduction in the Zener diodes and hence the dead time period produces losses, the duration of this period is much smaller compared to the other periods and hence losses in this period are neglected. Therefore the stored energy in the transformer at the end of the dead time period (t = t_2) is considered equal the energy at the end of the magnetisation period (t = t_3), hence (10);

$$E(t_2) = E(t_1) \quad (10)$$

Period 3 – t_2 to-t_3 – Demagnetisation period

With S1 and S2 OFF and S3 and S4 ON the sink capacitor C3 is connected across coil 2 of the transformer. The stored transformer energy can now be released via coil 2. Current is flowing through the multiplexer MOSFETs S3 and S4, the selector MOSFET ST2b and the anti-parallel diode D2a

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which are all conducting current during the demagnetisation period. The selector switch ST2a is not turned-on and its anti-parallel connected diode D2a is used to stop reverse current once the coil MMF has collapsed. Equations (11) to (14) describe the voltage and current waveforms for the demagnetisation period.

$$v_{L1}(t) = L_1 \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \quad (11)$$

$$v_{L2}(t) = -L_1 \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \quad (12)$$

$$i_{L1}(t) = 0 \quad (13)$$

$$i_{L2}(t) = I_{L1}(t_1) - \frac{V_{C3}}{5R_{ch} + R_D}\left(1 - e^{-\frac{5R_{ch}+R_D}{L_1}(t-t_2)}\right) \quad (14)$$

As coil 1 is still open circuit and coil 2 is connected to capacitor cell 3 the current level in coil 1 at the end of the magnetisation period $I_{L1}(t_1)$ appears as the initial current level at the start of the demagnetisation period as shown in equation (14). In order to drive the identical peak current at the beginning of the demagnetisation period the magnitude of the inductor voltage across coil 2 must be higher than the inductor voltage across coil 1 at the end of the magnetisation period;

$$|V_{L1}(\mathrm{t_1})| < |V_{L2}(\mathrm{t_2})| \quad (15)$$

This is because the voltage across coil 2, $v_{L2}(t)$, must be equal to the sum of the conduction voltages across the MOSFETs, the conduction voltage of the anti-parallel diode and the capacitor cell voltage, whereas in the magnetisation period the voltage across coil 1, $v_{L1}(t)$, is the sum of the cell voltage minus all the conduction voltage drops.

A higher secondary voltage with equal currents results in the instantaneous power output being higher than the instantaneous power input during magnetisation. Therefore, to satisfy conservation of energy the demagnetisation conduction time must be shorter than the magnetisation conduction time; (t_3-t_2) < (t_1-t_0). The energy during the demagnetisation period must be equal to the energy during the magnetisation period thus:

$$E = \int_{t_0}^{t_1} |v_{L1}(t) i_{L1}(t)|\,\mathrm{d}t = \int_{t_2}^{t_3} |v_{L2}(t) i_{L2}(t)|\,\mathrm{d}t \quad (16)$$

Period 4 – t_3 to-t_4 – Non-conduction period

When the MMF in the coil falls to zero there is no coil voltage and diode D2a stops any reverse conduction. Although the switches are all still on in the non-conduction period no current is flowing. All switches are turned off eventually in this period. Simulation and practical results show that a turn-off time of 500ns before the end of the time period T is sufficient.

III. Converter Control and Simulation

The principal operations of the converter described above apply to energy transfers between any capacitors in an n-number connected capacitor bank. The multiplexer connects the required capacitors and the selector activates the correct coils depending on the coil current directions. The control states for the case C1 – C3 are shown in Table 1.

Table 2 illustrates the switching states employed by the controller for any given combination of source and sink cells. Column 1 lists all combinations of source and sink capacitors depending on the order in the capacitor stack (odd or even number). Column two shows the voltage polarity across coil 1 during the magnetisation t_0–t_1 and demagnetisation period t_2–t_3. Column three shows the appropriate switching states for the magnetisation period t_0–t_1 and the demagnetisation period combined with the non-conduction period t_2–t_4.

Table 1 – Switching states of converter for energy passing from C1 to C3 (*all switches are turned off 500ns before the end of each switching period)

Switch	Time period			
	$t_0 - t_1$	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$
S1	1	0	0	0
S2	1	0	0	0
S3	0	0	1	1*
S4	0	0	1	1*
S5	0	0	0	0
S6	0	0	0	0
ST1a	1	0	0	0
ST1b	0	0	0	0
Sta2	0	0	0	0
STb2	0	0	1	1*

Table 2 – General switching states for any combination of energy flow paths

Where source cell is Cn and sink cell is Cm	Voltage polarity across coil 1		Active switches	
	$t_0 - t_1$	$t_2 - t_4$	$t_0 - t_1$	$t_2 - t_4$
n = odd m= odd	+ve	+ve	S(n), S(n+1), ST1a	S(m), S(m+1), ST2b
n = odd m = even	+ve	-ve	S(n), S(n+1), ST1b	S(m), S(m+1), ST1a
n = even m = odd	-ve	+ve	S(n), S(n+1), ST2a	S(m), S(m+1), ST2b
n = even m = even	-ve	-ve	S(n), S(n+1), ST2a	S(m), S(m+1), ST1b

For the purposes of proof of concept of the equalisation circuit a simulation model was developed in both SaberRD and PLECS. The capacitor cell model is based on the 2200F Li-Ion pouch cell prototypes with a datasheet nominal series resistance of around 1.5mΩ. Self-discharge effects are not considered. All internal resistance values have been taken from datasheets. The transformer was modelled using a pair of inductors coupled through a linear core (assuming no saturation) with an ideal coupling coefficient. The magnetisation period was fixed to half the switching time period; $(t_0 - t_1) = \frac{1}{2f}$, operating the converter with its maximum duty cycle of 50%.

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The simulation parameters for the components are listed in Table 3.

Table 3 – Simulation parameters

Parameter name	Value
MOSFET resistance	44mΩ
Selector diode resistance	1mΩ
Zener diode resistance	0.4mΩ
Converter switching frequency (f)	4kHz
Primary and secondary winding inductances	6µH 20µH 44µH
Winding coupling coefficient	1
Cell capacitance	2200F
Cell capacitor equivalent series resistance	1.5mΩ
Dead time period ($t_1 - t_2$)	500ns
Magnetisation period ($t_0 - t_1$)	125µs
Zener diode voltage	8.2V

The operation based on a circuit balancing 5 Li-Ion capacitors has been simulated. Figure 5 shows simulated waveforms for the converter operating at 4kHz with the primary winding inductance of L1=44µH. The voltage $v_{L1}(t)$ and $v_{L2}(t)$ are fully symmetrical as expected. During the magnetisation period both voltages drop over time. That is because the raising current $i_{L1}(t)$ produces an increasing voltage drop across the MOSFETs S1, S2, ST1a and the selector diode D1b. Likewise a voltage drop in the demagnetisation period is observed. The simulation in Fig. 5 shows further that the demagnetisation process is much shorter than the magnetisation process as explained earlier.

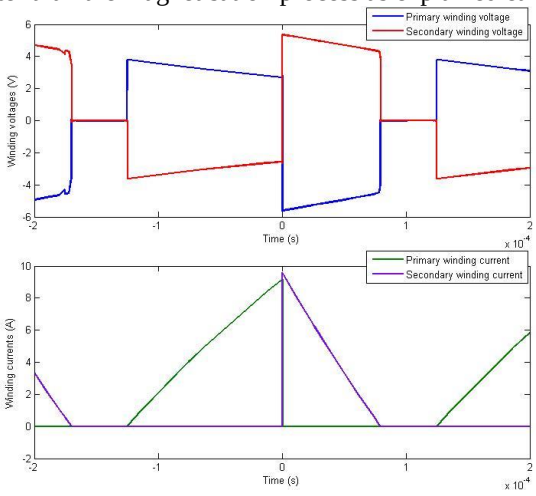

Figure 5 – Simulated converter voltage and current waveforms, f = 4kHz, L1 = 44uH. Top: coil voltages. Bottom coil currents

The simulation model was running over 20s comparing the rate of cell voltage change which is an important characteristic for active voltage balancing circuits. The change was measured for three inductance values: 6µH, 20µH and 44µH.

Figure 6 shows the merging of the two capacitor voltages V_{C1} and V_{C3} over 20 seconds (switching begins at t = 1s and ends at t = 19.5s) for L=44uH. The starting voltage for V_{C1} is 3.7V and for V_{C3} is 3.65V. The figure neglects the transient voltage drop across the internal resistance of the capacitor cells for clarity.

Figure 7 shows the cell voltages merging over the same time period with a 20µH primary winding and Figure 8 shows equalisation over the same period with a 6µH primary winding. Switching ceases at t = 16.5s after the two voltages have merged.

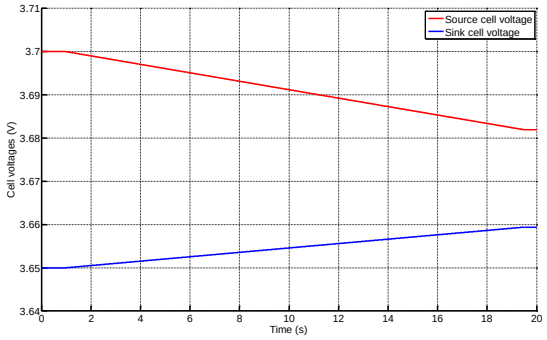

Figure 6 - C1 and C3 being equalised over 20s; f = 4kHz, L1 = 44µH

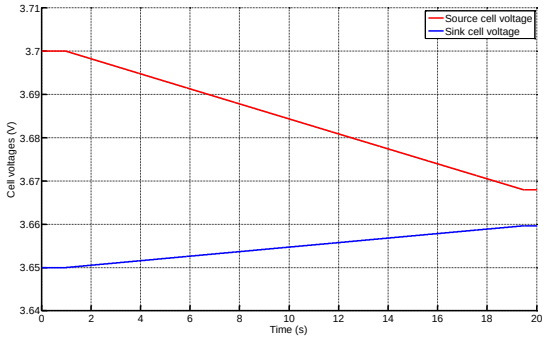

Figure 7 - C1 and C3 being equalised over 20s; f = 4kHz, L1 = 20µH

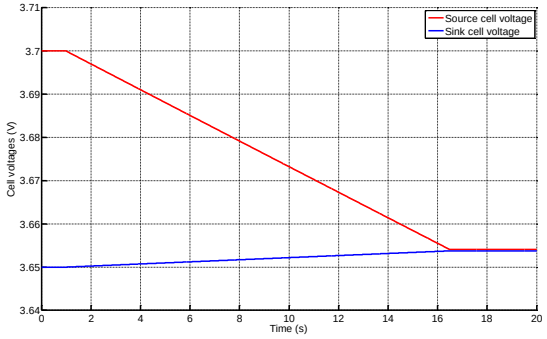

Figure 8 - C1 and C3 being equalised over 20s; f = 4kHz, L1 = 6µH

Figures 6-8 show that discharging of the source cell C1 is quicker than charging of the sink cell C3. This is the effect that the magnetisation period takes longer than demagnetisation period. This is due to the losses in the converter whereby not all energy which is released from the

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source cell is delivered to the sink cell and would be an effect of loss in all equalisation converters.

Table 4 compares the rate of cell voltage change factor (RCVC) -which is a measure in the speed of equalising different cell voltages- and the maximum coil current $i_{L1}(t = t_1)$. RCVC is expressed as the change of the voltage difference prior and after equalisation over the equalisation time:

$$RCVC = \frac{\Delta V_{before\ equlisation} - \Delta V_{after\ equlisation}}{\text{equlaisation time}} \quad (17)$$

For example, from Figure 6:

$$\Delta V_{before\ equlisation} = V_{C1}(t = 1s) - V_{C3}(t = 1s) = 3.7V - 3.65V = 0.05V \quad (18)$$

and

$$\Delta V_{after\ equlisation} = V_{C1}(t = 19.5s) - V_{C3}(t = 19.5s) = 3.682V - 3.659V = 0.023V \quad (19)$$

The equalisation time is 19.5s - 1s = 18.5s, thus RCVC = 1.46mV/s.

Table 4 – Simulated equalisation rate for each winding inductance

Inductance (µH)	RCVC (mV/s)	Maximum coil current $i_{L1}(t = t_1)$ (A)
6	3.2	22
20	2.3	14
44	1.5	8.5

IV. Operational Measurements

A prototype converter has been constructed and operated to demonstrate the principle of operation. A photograph of this prototype is shown in Figure 9.

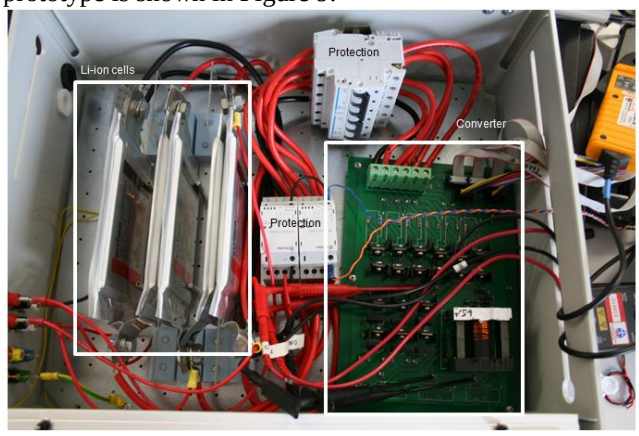

Figure 9 - Photograph of converter

For the purposes of technology demonstration a prototype has been constructed with a total of five cells (maximum stack voltage of 19V) but to the specification of a system containing 20 cells (a maximum 76V stack). This corresponds to a module specification for a commercial application.

For the converter the MOSFET switches IRF540N have been used for both the multiplexer switches and the selector switches. The IRF540N has high current capability (33A continuous) and low on state resistance (44mΩ). They are driven using HCPL-316 gate drive chips powered by 15V Traco Power TMR 3-2423 isolated DCDC converters. As is the case all previously presented equalisation schemes which have active switching components (with the exception of the one shown in Figure 1(a)) the switches in the proposed circuit 'float' relative to the stack ground since they are connected to different nodes along the cell stack. There is therefore a requirement in each of these circuits for gate drivers which have isolated supplies. Since this requirement is not singular to this circuit solution it does not represent an increased cost compared to existing circuits.

Various methods have been proposed in literature for multiplexing measurement of the cell voltage to the controller [25-27]. For simplicity in the case of the technology demonstrator described in this paper the differential voltage measurement of the cells is achieved using the AD629 high common mode rejection difference amplifier. The converter control is achieved using the Microchip 33FJ64GS610 dsPIC; a 16-bit 50MIPS architecture. This model processor has eight pairs of independent PWM channels which have individually addressable frequency, duty and phase values. The total of 12 required independent PWM channels required for the prototype leaves four spare channels. The control signals for all MOSFETs are created by using the master PWM counter. Figure 11 shows the schematic of the circuit.

For the purposes of analysis of the proposed equalisation scheme the operation of the hardware described above is identical to that of the simulated system described in section III whereby equalisation takes place between the first and third cells on the stack.

Figure 10 shows the measured voltage and current waveforms for the circuit in operation with a switching frequency of 4kHz and a winding inductance of 44µH.

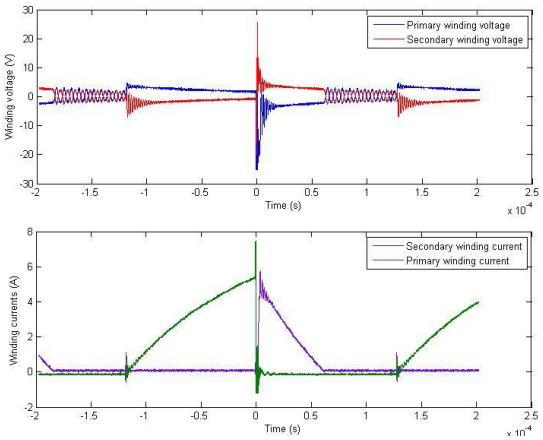

Figure 10 – Measured converter voltage and current waveforms, f = 4kHz, Lp = 44uH

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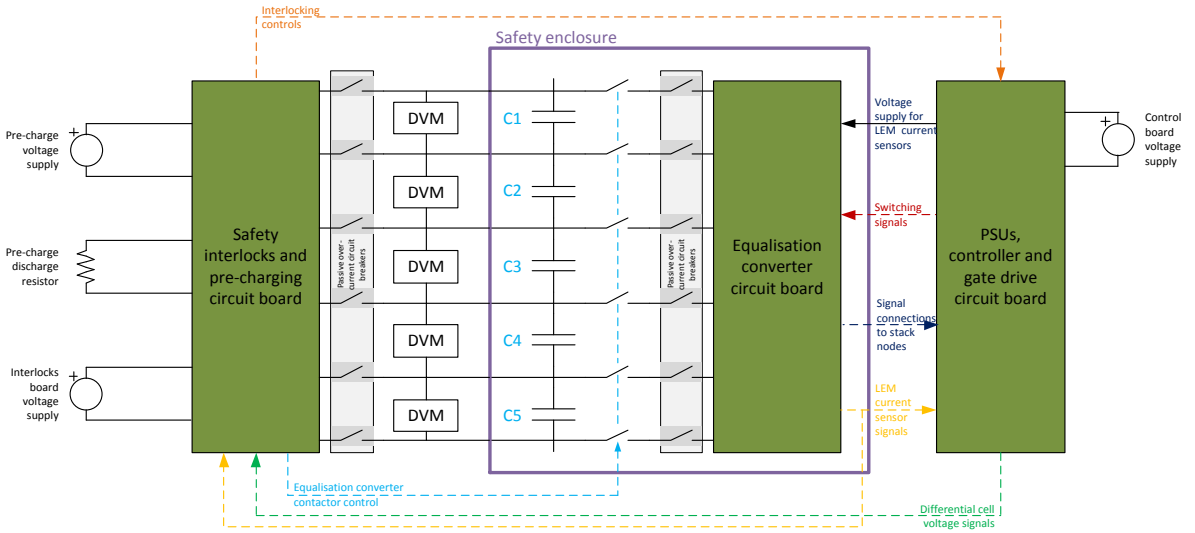

Figure 11 - System level diagram of experimental apparatus

Comparing the results to the simulated results in section III shows that the peak current is lower than predicted in the simulations. The appearance of voltage oscillation ringing during the non-conduction period is another difference to the simulated data. The reduction in current is explained first. Figure 12 shows a magnified image of the waveforms during the magnetisation period. As shown in Figure 12, at a time just before the commutation point the instantaneous primary winding current is approximately 5.2A. The corresponding drop in voltage applied to the primary coil – which is a result of the conduction voltage drops of the MOSFET switches S1, S2, ST1a and the anti-parallel diode D1b as described in (3) – is approximately 2V. The series resistance of the conduction loop, excluding any resistance of the coil since the voltage is measured across it, can therefore be calculated using Ohm's law as 380mΩ. This value is higher than the value of around 220mΩ which was calculated from the hardware datasheets of the MOSFET switches and the diode. The explanation for this increased series resistance lies in the added resistance of the protection circuit breakers (Figure 11) which, although essential for prototype commissioning and testing would not be present in a more developed version of the hardware.

The missing oscillation in the simulation can be explained because the simulated system employs an idealised transformer with no capacitance modelled. As an approximation, a small parallel capacitance added to each of the transformer windings may be used to model winding capacitance.

Figure 13 shows simulated results based on the additional resistance of the circuit breaker and adding parasitic capacitances of 20nF across the transformer. These waveforms match more closely the measured results.

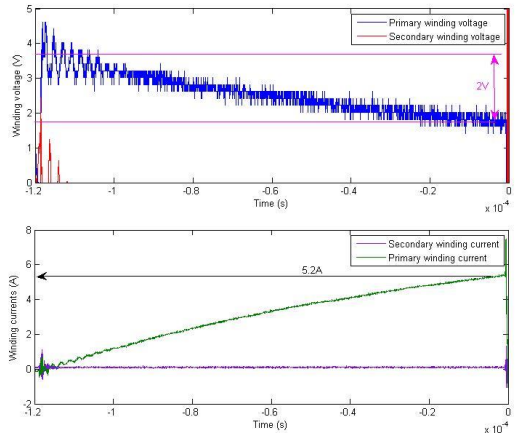

Figure 12 - Analysis of voltage drop during magnetisation. f = 4kHz, Lp = 44µH

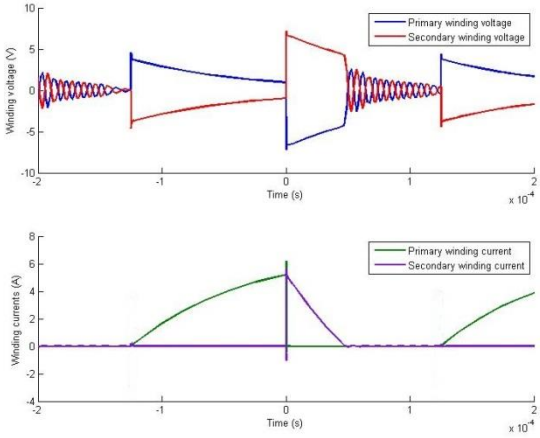

Figure 13 - Adjusted simulation results for greater series resistance and added parasitic transformer winding capacitances

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The equalisation converter has been operated with three values of inductance (6, 20 and 44µH) over 20s. Table 5 shows the rate of cell voltage change factor (RCVC) and the maximum peak current in coil 1.

Table 5 - Equalisation rate for each winding inductance

Inductance (µH)	RCVC (mV/s)	Maximum coil current $iL_1(t = t1)$ (A)
6	2.1	10
20	1.4	8.4
44	1.1	5.2

Figures 14-16 show the equalisation converter performance using 44, 20 and 6µH primary winding respectively. The equalisation performance shows that two cell voltages do indeed converge as predicted however, as would be expected from the increased resistance, more slowly.

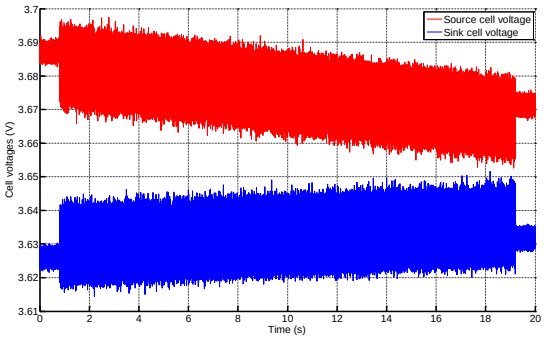

Figure 14 - Voltage equalisation over 20s. f = 4kHz, L_1 = 44µH

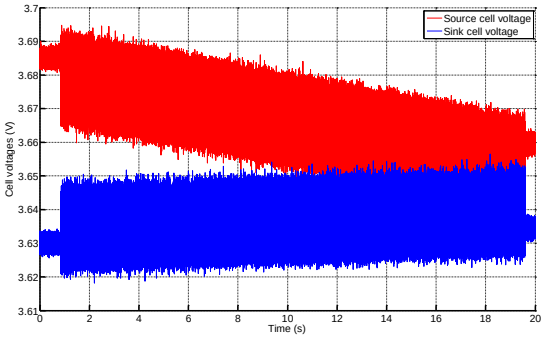

Figure 15 - Voltage equalisation over 20s. f = 4kHz, L_1 = 20µH

Comparing all three figures it can be concluded that a lower coil inductance show better performance in terms of rate of cell voltage changes. Faster convergence will be achieved by eliminating the prototype circuit breakers and choosing MOSFETs and diodes with lower on-state resistances.

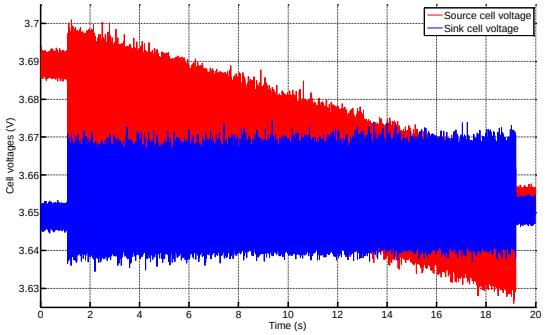

Figure 16 - Voltage equalisation over 20s. f = 4kHz, L1 = 6µH

V. Conclusion

Transformer-based active voltage balancing circuits have become an attractive solution for efficient voltage balancing for in series connected capacitance devices such as Li-Ion capacitors. However, multi-winding transformers are not feasible for a large number of in series connected capacitor cells. A new converter topology is presented that allows the use of a classical two windings transformer utilising a multiplexer and a selector circuit. This circuit can be applied to any number of capacitors in series.

The performance of the proposed circuit is analysed and has been explored through simulation. The proposed equalisation converter has been constructed and tested and shown to operate almost as expected. Some behaviour, such as the voltage ringing, has been attributed to parasitic effects of the prototype as constructed and further study may allow for the mitigation of these effects.

The proposed converter has a relatively good equalisation rate when operating in conjunction with the cells of the capacity used for this work. Equalisation rate is dependent on the losses in the equalisation circuit and the capacity of the cells in the stack. The equalisation of the presented converter could be improved when implementing switching devise with lower internal resistances.

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